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Amendments to the Claims

1. (Currently Amended) A method for forming short-channel transistors, comprising the steps of:

forming a first oxide layer and a sacrificial layer one after another on a semiconductor substrate and etching the sacrificial layer, thus forming a residual sacrificial layer pattern;

conducting an ion implantation using the residual sacrificial layer pattern as a mask, thus forming an LDD ion-implant layer in the semiconductor substrate;

forming first spacers on both side walls of the residual sacrificial layer pattern;

conducting an ion implantation using the residual sacrificial layer pattern and the first spacers as a mask, thus forming a source/drain ion-implant layer under the LDD ion-implant layer;

forming a nitride layer and a second oxide layer one after another on the whole surface of the former resultant object and conducting an annealing treatment, thus forming source/drain regions;

conducting a chemical-mechanical polishing (CMP) process to the extent that an upper surface of the residual sacrificial layer pattern is exposed, and removing the residual sacrificial layer pattern through etching;

forming second spacers on side walls of a portion where the residual sacrificial layer pattern is removed;

conducting an ion implantation on the substrate between the second spacers and through the first oxide layer, thus forming a punch-stop ion implant layer;

etching the first oxide layer under the portion where the residual sacrificial layer pattern is removed, and forming a gate insulation layer having a thickness sufficient to reach the second spacers; and

forming a gate on the second spacers and the gate insulation layer where the residual sacrificial layer pattern is removed.

2. (Original) The method for forming short-channel transistors as claimed in claim 1, wherein upon etching the sacrificial layer, the first oxide layer is used as an etch stopper layer.

3. (Original) The method for forming short-channel transistors as claimed in claim

1, wherein the gate insulation layer and the gate are formed after the source/drain regions are previously formed.

4. (Previously Presented) The method for forming short-channel transistors as claimed in claim 1, wherein the sacrificial layer consists essentially of polysilicon.

5. (Original) The method for forming short-channel transistors as claimed in claim 1, wherein the second oxide layer is multi-layered.

6. (Original) The method for forming short-channel transistors as claimed in claim 1, wherein the punch-stop ion implant layer is adapted as a threshold-voltage adjustment ion implant layer.

7. (Original) The method for forming short-channel transistors as claimed in claim 1, wherein upon ion implantation of LDD and the source/drain, the first oxide layer is used as a buffer layer for ion implantation.

8. (Previously Presented) The method for forming short-channel transistors as claimed in claim 1, wherein the first and second spacers comprise the same materials.

9. (Previously Presented) The method for forming short-channel transistors as claimed in claim 1, wherein the first and second spacers each consist essentially of a nitride layer.

10. (Previously Presented) The method for forming short-channel transistors as claimed in claim 8, wherein the first and second spacers each consist essentially of a nitride layer.

11. (Previously Presented) The method for forming short-channel transistors as claimed in claim 1, wherein the sacrificial layer consists essentially of polysilicon.

12. (Previously Presented) The method for forming short-channel transistors as claimed in claim 1, wherein removing the residual sacrificial layer pattern comprises wet etching the residual sacrificial layer pattern.

13. (Previously Presented) The method for forming short-channel transistors as claimed in claim 1, wherein upon etching the residual sacrificial layer pattern, the first oxide layer is used as an etch stopper layer.

14. (Currently Amended) A method for forming short-channel transistors, comprising the steps of:

on a semiconductor substrate having a first oxide layer thereon, a residual sacrificial layer pattern on the first oxide layer, first spacers on side walls of the residual sacrificial layer pattern, an LDD ion-implant layer in the semiconductor substrate not masked by the residual sacrificial layer pattern, a source/drain ion-implant layer under the LDD ion-implant layer not masked by the first spacers, and a nitride layer and a second oxide layer on the surface thereof, removing the residual sacrificial layer pattern by etching, using the first oxide layer as an etch stopper;

forming second spacers on side walls of the first spacers;

forming a punch-stop layer on the substrate by ion implantation between the second spacers and through the first oxide layer;

etching the exposed first oxide layer, and forming a gate insulation layer having a thickness sufficient to reach the second spacers; and

forming a gate on the gate insulation layer and the second spacers.

15. (Previously Presented) The method for forming short-channel transistors as claimed in claim 14, further comprising, prior to the residual sacrificial layer pattern removing step, chemical-mechanical polishing the nitride layer and second oxide layer to planarize the nitride layer and second oxide layer and expose an upper surface of the residual sacrificial layer pattern.

16. (Previously Presented) The method for forming short-channel transistors as claimed in claim 14, wherein the sacrificial layer consists essentially of polysilicon.

17. (Previously Presented) The method for forming short-channel transistors as claimed in claim 14, wherein the first spacers consist essentially of a nitride layer.

18. (Previously Presented) The method for forming short-channel transistors as claimed in claim 17, wherein the second spacers consist essentially of a nitride layer.

19. (Previously Presented) The method for forming short-channel transistors as claimed in claim 14, wherein the gate forming step comprises depositing a polysilicon layer on a whole surface of a structure following the gate insulation layer forming step, and planarizing the polysilicon layer to form the gate.

20. (Currently Amended) The method for forming short-channel transistors as claimed in claim [[14]]19, wherein the sacrificial layer consists essentially of polysilicon.